PROCESS CP257

Small Signal Transistor

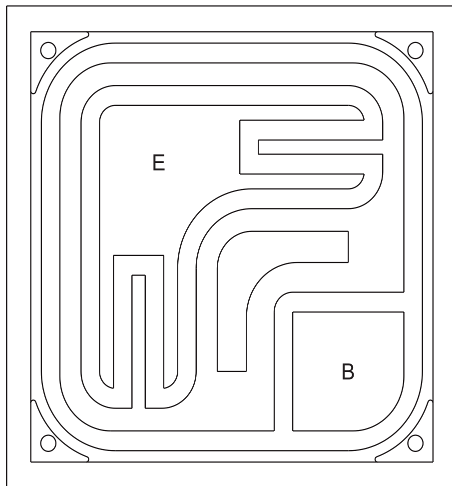
NPN - High Voltage Darlington Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	20 x 20 MILS
Die Thickness	8.0 MILS
Base Bonding Pad Area	4.9 x 4.9 MILS
Emitter Bonding Pad Area	6.4 x 6.4 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 16,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 4 INCH WAFER
28,250

PRINCIPAL DEVICE TYPES
MPSA28
MPSA29
CMPTA29

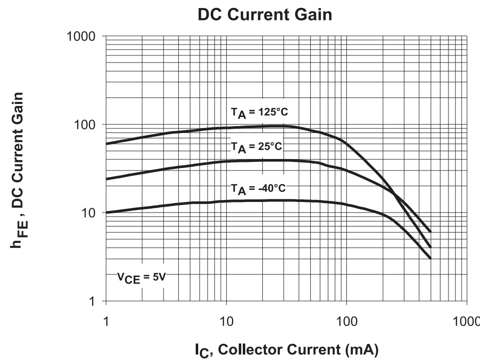
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

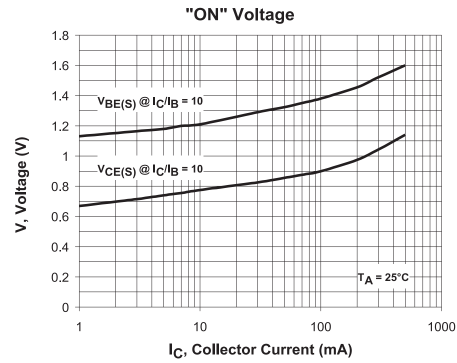
R3 (21-September 2003)

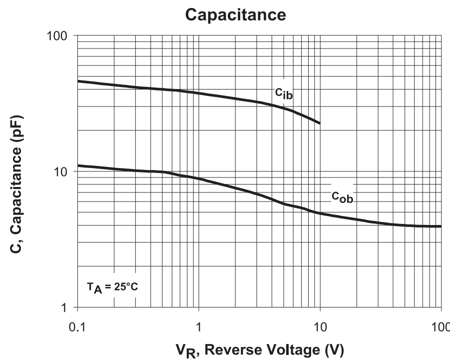
Central™
Semiconductor Corp.

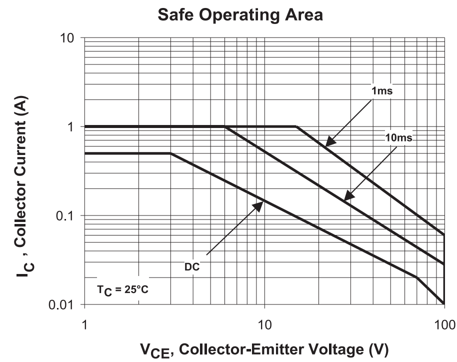
PROCESS CP257

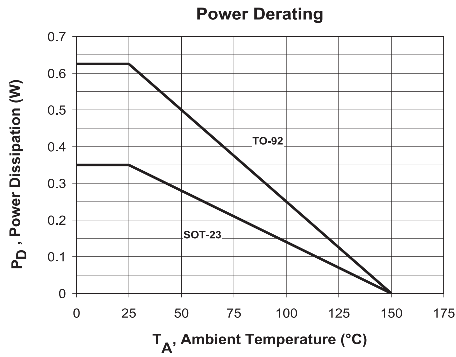
Typical Electrical Characteristics

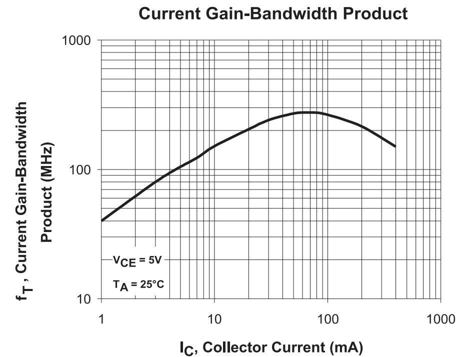












145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R3 (21-September 2003)